CLAIMS

1. A method for establishing a master unit in a parallel system including multiple modules connected in parallel, characterized in that each module in said parallel system is marked with a respective number and connected through at least one contention bus, wherein the modules with said respective numbers have different host-identifying pulse width (Ts) and host releasing pulse width (Tw); each of said modules sending the corresponding host-identifying pulse to said contention bus according to its number and receiving a feedback pulse from said contention bus at the same time; and one of said modules being established as a master unit by comparing its received feedback pulse width (Tr) with its host-releasing pulse width (Tw).

2. The method of claim 1, characterized in that said contention bus is a logic OR bus, each of said modules being initially defaulted as a slave unit, and each of said modules sending an invalid low level to said contention bus.

3. The method of claim 2, characterizedin that each of said modules sends a host-identifying pulse to said contention bus to ensure the uniqueness of the master unit, comprising the following steps: setting any of the modules that has not started or been turned off as a slave unit; the module that has started sending its host-identifying pulse to said contention bus and detecting the feedback pulse width (Tr); setting the module as master unit if the feedback pulse width (Tr) is smaller than its host-releasing pulse width (Tw); and setting the module as the slave unit if the feedback pulse width (Tr) is larger than its host-releasing pulse width (Tw).

4. The method of claim 1, characterized in that said contention bus comprises a first contention bus and a second contention bus, each of said modules being initially defaulted as a slave unit, and each of said modules sending an invalid low level to said first and second contention buses.

5. The method of claim 4, characterized in that each of said modules sends a low level to the first contention bus in order to ensure the existence of the master unit, comprising the following steps: setting any of the modules that has not started up or been turned off as a slave unit; all the modules that

act as slave units sending low levels to said first contention bus, while the module that serves as the master unit sending a high level to said first contention bus; each of said modules that has started detecting the feedback pulse from said first contention bus, and setting the module as the master unit if the feedback level is low; maintaining the module as the slave unit if the feedback level is high and the module is a slave unit; if the feedback level is high and the module is set as a master unit, each of said modules performing a further step to send the corresponding host-identifying pulse to the second contention bus to ensure that the master unit is unique.

6. The method of claim 5, characterized in that each of said modules sends its host-identifying pulse to the second contention bus in order to ensure the uniqueness of the master unit, comprising the following steps: all of the modules that act as slave units sending low levels to said second contention bus, while the module that serves as the master unit sending a periodical host-identifying pulse to said second contention bus according to its number; each of said modules detecting the feedback pulse from said second contention bus and recording the feedback pulse width (Tr) in real time; if the feedback level from said first contention bus detected by said each module is high and the module is set as a master unit, and if the feedback pulse width (Tr) from the second contention bus is smaller than the host-releasing pulse width (Tw) of the module, maintaining the module as the master unit; otherwise releasing the module from the master state and setting the module as a slave unit.

7. The method of claim 6, characterized in that said first contention bus and said second contention bus are simple logic OR bus or simple AND bus.

8. The method of claim 7, characterized in that each of said modules sends logic level to said first contention bus by using a first contention logic associated with said first contention bus; each of said modules sends the host-identifying pulse to said second contention bus and detects said second contention bus by using a second contention logic associated with said second contention bus; said first contention logic and said second contention logic can be realized by a digital circuits, such as a trigger based circuits, or a microprocessor and programmable logic device.

9. The method of any of claim 1-8, characterized in that the number of each of said modules corresponds to a priority; the host-identifying pulse width (Ts) of the module with a high priority is larger than the sum of the host-identifying pulse width (Ts) of the modules with lower priorities, and is larger than the host-releasing pulse width (Tw) of any of the modules with a lower priority; the host-releasing pulse width (Tw) of each module other than the one with the highest priority is larger than the host-identifying pulse width (Ts) of the module, at the same time, the host-releasing pulse width (Tw) is larger than the host-releasing pulse width (Tw) of the modules with lower priorities.